Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A IN**
2. **1B IN**
3. **N/C**
4. **1C IN**
5. **1D IN**
6. **1Y OUT**
7. **GND**
8. **2Y OUT**
9. **2A IN**
10. **2B IN**
11. **N/C**
12. **2C IN**
13. **2D IN**
14. **VCC**

**.041”**

**2 1 14 13**

**3**

**4**

**5 6 7 8 9**

**12**

**11**

**10**

**MASK**

**REF**

**C L**

**S 2**

**R 0**

**.035”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: LSR20 C**

**APPROVED BY: DK DIE SIZE .035” X .041” DATE: 8/18/21**

**MFG: NATIONAL THICKNESS .021” P/N: 54LSR20 / 54LS20**

**DG 10.1.2**

#### Rev B, 7/1